REMARKS

The examiner rejected claims 1-23 under 35 U.S.C. 102(b) as being anticipated by Chang et al US Patent 5,634,015.

Claims 1-23 as amended are distinct over Chang. Claim 1, as amended, recites a method that includes... storing queue descriptors in a memory, determining which of the queue descriptors stored in the memory were most recently accessed according to a criterion, and storing the determined subset of queue descriptors in a cache in a processor's memory controller logic, the determined subset of queue descriptors stored in the cache including less than all of the queue descriptors stored in the memory.

Chang stores system packets in a packet memory. Due to the length of a particlular packet, the packet may be partitioned into multiple buffers within the memory. Two memories (GAM 18 and GAM local memory 30) are used to track the location of the packet data in the memory. The GAM 18 is used to track the packets and "the GAM has one packet table entry (PTE) in its local memory for each existing packet in the PM" (emphasis added, col. 17, lines 60-63). Since the packet may have been divided into multiple buffers, the GAM local memory 30 tracks the multiple buffers for each packet. "For each buffer in the packet memory (PM) there is one corresponding buffer table entry in the GAM local memory 30" (emphasis added, col. 17, lines 24-26). Since Chang stores an entry for each packet in the GAM and one or more entries for each packet in the GAM local memory, neither the GAM nor the GAM local memory disclosed in Chang can not be equivalent to the cache in the applicant's claim 1.

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Chang neither describes nor suggests modifying the structure and storage of the packet descriptors to determine which of the queue descriptors stored in the memory were most recently accessed according to a criterion, and store the determined subset of queue descriptors (the subset including less than all of the queue descriptors) in a cache in a processor's memory controller logic. Thus, Chang does not anticipate the applicant's claim 1.

For at least the same reasons, applicant submits claim 1 should be allowed, applicant submits that dependent claims 2-8 should be allowed.

Claim 9 distinguishes by reciting a "memory controller logic that includes a cache to store a subset of the queue descriptors in the memory, the subset determined based on which of the queue descriptors stored in the memory were most recently accessed according to a criterion." Thus, based on these limitations claim 9 is patentable for reasons similar to claim 1.

For at least the same reasons, applicant submits claim 9 should be allowed, applicant submits that dependent claims 10-15 should be allowed.

Claim 16 includes instructions causing a computer to "store queue descriptors in a memory, the queue descriptors each specifying a structure of a respective queue, determine which of the queue descriptors stored in the memory were most recently accessed according to a criterion, [and] store the determined a subset of queue descriptors in a cache in a processor's memory controller logic." Thus, based on these limitations claim 16 is patentable for reasons similar to claim 1.

For at least the same reasons, applicant submits claim 16 should be allowed, applicant submits that dependent claims 17-23 should be allowed.

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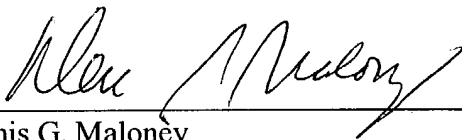
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The fact that the applicant has addressed certain comments of the examiner does not mean that the applicant concedes any other positions of the examiner. The fact that the applicant has asserted certain grounds for the patentability of a claim does not mean that there are not other good grounds for patentability of that claim or other claims.

Please apply any charges or credits to deposit account 06-1050, referencing Attorney Docket No. 10559-610001.

Respectfully submitted,
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